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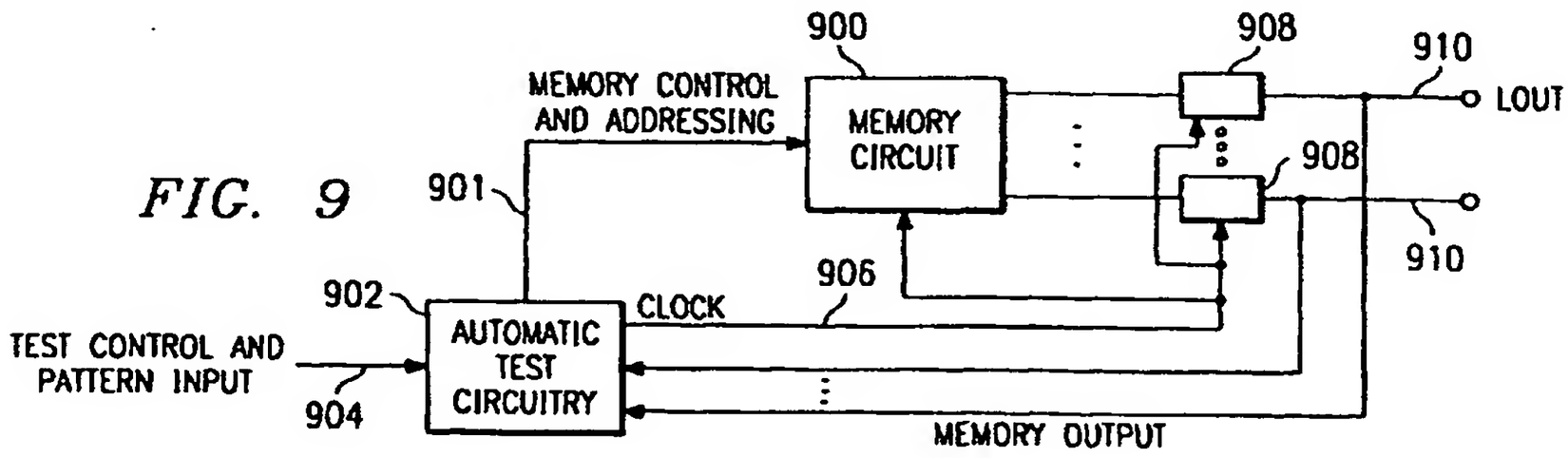
(54) Memory access time measurement circuit and method

(57) A circuit for measuring the access time of a memory circuit. The circuit includes a storage element 908 having an input terminal, an output terminal, and a clock terminal. The input terminal of the storage element is coupled to an output of the memory circuit 900. A clock signal source 906 is coupled to the clock terminal of the storage element and to a clock terminal of the memory circuit. The circuit also includes test circuitry 902 coupled to address and control terminals of the memory circuit and to the output terminal of the storage element. The test circuitry is operable to store or generate a test data pattern and compare the pattern to data output from the storage element. In one embodiment, the storage element is a data latch comprising a clock-enabled inverter serially coupled with a flip-flop. The flip-flop in one embodiment is a cross-coupled inverter storage cell or "keeper". For a clock signal having a pulse length or duty cycle that is longer than the access time of the memory circuit, the output of the storage element matches the data pattern stored by the test circuitry. As the clock frequency is increased, or the duty cycle decreased, so that the pulse length approximates the access time, the data output from the storage element no longer matches the data expected by the test circuitry, thus allowing a determination of the access time.

FIG. 9



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Description

FIELD OF THE INVENTION

The present invention generally relates to electronic circuits, and more specifically to a circuit and method for measurement of access time of a memory circuit.

BACKGROUND OF THE INVENTION

The measurement of access time in memory circuits is one of the most difficult items in integrated circuit testing. Access time is generally defined as the delay between the inputting of information to a memory circuit and the presence of valid data at the output of the memory circuit. One common parameter is the address access time, that is, the amount of delay between providing a memory cell address and the availability of the store data at the output of the circuit. The address access times for static random access memory circuits (SRAMs) and dynamic random access memory circuits (DRAMs) are of the order of tens of nanoseconds. The brevity of the access time parameter is one factor in making the measurement difficult.

Techniques used in the past have typically relied on two or more clock signals to measure access time. This is particularly so for synchronous circuits, that is, memory devices in which the transfer of information into, within, and out of the circuit is coordinated with a clock signal. In one example of an access time measurement using multiple clocks, one clock signal is used to regulate the latching of address information and the propagation of signals within the memory circuit, while a second clock is used to regulate the outputting of data.

The multiple-clock approaches suffer from several problems. For example, die space is consumed by the pads and lines associated with additional clocks. Typically, the additional space on an integrated circuit die devoted to testing the integrated circuit is often referred to as "test overhead". In addition, in a system that relies on two or more clocks, the propagation delay differences between the clock signals may affect the accuracy of the access-time measurement. A need exists in the industry for a solution to these problems.

SUMMARY OF THE INVENTION

In accordance with a particularly preferred embodiment of the invention, there is disclosed a circuit for measuring the access time of a memory circuit. The circuit includes a storage element having an input terminal, an output terminal, and a clock terminal. The input terminal of the storage element is coupled to an output of the memory circuit. A clock signal source is coupled to the clock terminal of the storage element and to a clock terminal of the memory circuit. The circuit also includes test circuitry coupled to address and control terminals of the memory circuit and to the output terminal of the storage element. The test circuitry is operable to store a test data pattern, or alternatively to generate a test pattern, and compare the pattern to data output from the storage element. In one embodiment, the storage element is a data latch comprising a clock-enabled inverter serially coupled with a flip-flop. The flip-flop in one embodiment is a cross-coupled inverter storage cell or "keeper". For a clock signal having a pulse length or duty cycle that is longer than the access time of the memory circuit, the output of the storage element matches the data pattern stored by the test circuitry. As the clock frequency is increased, or the duty cycle decreased, so that the pulse length approximates the access time, the data output from the storage element no longer matches the data expected by the test circuitry, thus allowing a determination of the access time.

An advantage of the inventive concepts is that an access time measurement is possible using a single clock signal. Thus, the test overhead on the integrated circuit is kept to a minimum and problems with differing delays between clock signals are avoided. In addition, no extra package pins or terminals are required by the measurement approach.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described by way of example, with reference to the accompanying drawings in which:

Figure 1 is a block diagram of an integrated circuit having embedded memory and application-specific logic circuits;
Figure 2 is a timing diagram showing the synchronous operation of a memory circuit;
Figure 3 is a block diagram of a first preferred embodiment circuit;
Figure 4 is a schematic diagram of a latch circuit that may be used in conjunction with the circuit of Figure 3;
Figure 5 is a block diagram of an alternative approach to that shown in Figure 3;
Figures 6a-6f are alternative latch schemes to that shown in Figure 4;
Figures 7a to 7c are timing diagrams showing operation of the embodiment;
Figures 8a to 8c are timing diagrams showing operation of the embodiment measurement technique for non-uniform memory cell access times;
Figure 9 is a block diagram of an embodiment test circuit; and
Figure 10 is a block diagram of an embodiment memory integrated circuit.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the description of the illustrated preferred

embodiments of the invention that follow, an access time measurement is possible with a single clock signal. The techniques may be applied to both synchronous and asynchronous circuits and to DRAMs, SRAMs, and other types of integrated circuits such as those having clocked or synchronous input circuits and flow-through or nonsynchronous output circuits (flash memory and simple adders, for example). Figure 1 is a block diagram of how a single-clock access-time measurement technique that has been applied to an embedded DRAM module. In Figure 1, DRAM module 100 is integrated on a single semiconductor die 102 with application-specific integrated circuit (ASIC) logic module 104. ASIC module 104 may be a microprocessor, microcontroller, digital signal processor, or other logic circuit. The clock signal used to regulate the transfer of data into, within, and out of the DRAM is provided at clock terminal 106. Buffer driver 108 drives the data out of the DRAM circuit and into the receiver buffer 110 of the ASIC logic module 104. The access time measurement is made by sampling the output at data output monitor terminal 112. The signal from buffer driver 108 is enhanced by a test buffer driver 114.

The circuit of Figure 1 suffers from several problems. First, as depicted in Figure 1, it is typical that the receiver buffer 110 of the ASIC logic module 104 is near the middle of the integrated circuit die, while the monitor terminal 112 is near the edge of the die. The distance between the receiver and the monitor terminal 112 causes a signal propagation delay that results in error in the access time measurement. Even more delay in the test signal is induced by the additional driver 114 used to drive the test signal to the test equipment that is coupled to monitor terminal 112.

Figure 2 is a timing diagram of a synchronous DRAM. Signal (a) is an external clock signal applied during testing at terminal 106 in Figure 1, for example. Signals (b) and (c) are the complements of the row address and column address strobes, respectively, applied during testing at terminals 116 and 118 in Figure 1, for example. Signal (d) is the row and column address information input at a plurality of terminals 120 in Figure 1, for example. Of course, the DRAM module 100 and ASIC logic module 104 are connected by a bus 121 that carries control and address signals in the operating mode of the integrated circuit where address and control signals are provided to the memory module by the ASIC logic module. Only one row address (R0) and three column addresses (C0,C1,C2) are shown in line (d), but one skilled in the art will appreciate that many more or fewer address bits may be used. The signal in line (e) is the data output of the memory circuit. The first bits of the output (R0C0) are delayed by three clock cycles, hence the CAS latency is three in this example. The delay t_{AC} is the access time of the DRAM. The access time is measured from a rising edge of the clock signal, and is not influenced by a falling clock signal edge.

Figure 3 illustrates a particularly preferred embodiment circuit of the present invention. The block diagram of Figure 3 is similar to that of Figure 1, except that storage element or latch 322 is coupled between the output of the DRAM module 300 and the test monitor terminal 312. An example of a latch 322 is shown in Figure 4. The latch comprises an input terminal 400, an output terminal 402, and a clock terminal 404. P-channel transistor 408 and n-channel transistor 410 form an inverter that is enabled or disabled by transistors 406 and 412 in accordance with a clock signal at terminal 404. Inverters 416 and 418 form a storage cell or flip-flop core (in this embodiment a cross-coupled inverter storage cell) that stores the output of the inverter formed by transistors 408 and 410 until the output changes. The latch may be incorporated in the ASIC logic module 304 or in the DRAM module 300.

In operation, when the clock signal at terminal 404 is a logic high, transistors 406 and 412 are conductive and the transistors 408 and 410 act as a conventional inverter. For example, a logic high input at terminal 400 produces a logic low output at node 420. For a logic low input at terminal 400, the output at node 420 is a logic high. The signal at node 420 is stored by the storage cell that comprises inverters 416 and 418. The signal is retained by the storage cell until the logic level at node 420 changes. Inverter 416 also inverts the signal at node 420 such that a high logic level input at terminal 400, for example, produces a high logic level output at output terminal 402. The output terminal 402 remains at the high logic level until a low logic level appears at input terminal 400. When the clock signal is a logic low, transistors 406 and 412 are non-conductive, this tri-stating node 420. Therefore, during the low-voltage portion of the clock cycle, the output of the latch remains the same as the last data at the input terminal 400 during the logic high portion of the clock cycle.

A feature of the latch shown in Figure 4 is that it is made transparent by holding the voltage on the clock terminal 404 at a logic high. In this condition, a signal encounters only slight delay in passing through the latch. The latch can also be inactivated when the integrated circuit is in operating mode rather than test mode. By simply holding the clock terminal 404 at a logic low, the transistors 406 and 412 are inactivated, thereby disabling the inverter formed by transistors 408 and 410. This feature allows the portions of the integrated circuit of Figure 3 that are associated only with the testing of the circuit to be disabled so as to not interfere with the normal operations of the integrated circuit and to prevent unnecessary dissipation of power in the test circuits. The feature of the latch being transparent when the clock terminal is held at a logic high makes possible the alternative embodiment shown in Figure 5. In Figure 3, the latch occupies a shunt position relative to the memory module output 324. In Figure 5, however, the latch is in the data path from the memory module 500 to the ASIC logic module 504. With the clock termi-

nal 404 of the latch held at a logic high, the latch passes the data 524 with only slight delay. Holding the clock terminal low interrupts a data transfer on line 524.

One skilled in the art will appreciate that many comparable latches may be used other than the one shown in Figure 4. Examples of alternatives include those shown in Figures 6a through 6f.

The operation of the circuit of Figure 3 may be better understood by referring to Figures 7a, 7b and 7c. In Figure 7a, line (a) is the clock signal supplied at terminal 306 in Figure 3, for example. Line (b) is the data output of the DRAM module 300. Once a request is made of the memory module to provide data from a particular cell, a delay of t_{AC} (the access time of the memory) elapses before the data appears at the output 324 of the memory module. For example, in Figure 7a the address for location R0C2 is given to the memory module when the rising edge of the clock signal occurs at time t_1. Time t_{AC} elapses before the data for R0C2 appears at the output of the memory module. But since the falling edge of the clock signal occurs after the transition in line (b) from the R0C1 data location to the R0C2 data location, the latch 322 stores the current value of Dout on the falling edge of the clock cycle. In this example, the data Dout at the falling edge of the clock pulse that begins at t_1 is R0C2. Hence, in the situation shown in Figure 7a where the portion of the clock cycle that is a logic high voltage exceeds the access time period, the output of the latch 322, Lout, reflects the current value at the monitor point t_M, of the data output from the memory module 300.

In contrast, in Figure 7b a situation is shown in which the circuit of Figure 3 is clocked at a frequency in which the logic high portion of the clock cycle is shorter than the access times of the cells in the memory module. Therefore, at the falling edge of the clock pulse that begins at t_1, the data for R0C1 still appears at the output even though the data for R0C2 was requested in time t_1. Since the falling edge of the clock occurs when R0C1 was at the input to latch 322, R0C1 is stored until the clock goes low with R0C2 on the latch input. In summary, when the clock frequency is fast enough that the logic high portion of the clock cycle (the clock pulse) is shorter than the memory access time, the latch stores the data of the previous requested memory location. But when the pulse length is longer than the memory access time, the latch stores the data of the currently requested memory location (when Dout and Lout are compared at time tM). This is true for locations having relatively uniform access times. Figures 8a to 8c show a situation where cell access times are nonuniform.

Figure 7c illustrates that a similar result to that in Figure 7b can be obtained by simply decreasing the duty cycle of the clock pulse while keeping the clock frequency constant. As in Figure 7b, the falling edge of the pulse that begins at t_1 occurs with R0C1 is active on line (b), even through the R0C2 data was requested at time t_1.

Figures 7a to 7c show a situation where the access times of the memory cell locations R0C0, R0C1 and R0C2 are approximately equal. Thus, in Figures 7b and 7c, all of the Lout data for cell locations R0C0, R0C1 and R0C2 is out of phase with the Dout data for the clock frequency variation shown in Figure 7b and for the clock duty cycle variation shown in Figure 7c. Even though all of the latched data for R0C0, R0C1 and R0C2 is out of phase with the Dout data, all of the Dout data is latched. The situation is different when the access times for data locations are substantially different.

Figures 8a to 8c show a situation where the access times of the memory cell locations are not approximately equal. Specifically, in line (b) of Figure 8a, the access time, t_{AC1}, of cell R0C2 is much longer than the access time, t_{AC2} of cell R0C3. At the frequency and duty cycle of the clock signal in line (a), inspection of line (c) shows that all of the data, Dout, in line (b) is latched. A comparison of the phases of the Dout and Lout datastreams however, may not be as valuable as in the situation described in Figures 7a to 7c where the access times of the data cells were relatively uniform. As can be seen in Figures 8b and 8c, when the clock frequency is increased (Figure 8b) or the duty cycle decreased (Figure 8c), not all of the Dout data is latched. Indeed, the access time, t_{AC1} of location R0C2 is long enough and the access time of location R0C3 is short enough that the data for R0C2 is not latched. Thus, the sequence of Lout data in Figure 8b is R0C0, R0C1, R0C3, rather than R0C0, R0C1, R0C2, R0C3 as shown in Figure 8a. Figure 8c shows that a similar result can be obtained by decreasing the duty cycle of the clock signal while holding the frequency constant.

The phenomena described above can be used to measure access time. An embodiment block diagram of a test system to measure access time is shown in Figure 9. One skilled in the art will appreciate that testing can be accomplished with test circuitry external to the integrated circuit or with built-in self test (BIST) circuitry on the same semiconductor die as the circuit to be tested. The automatic test circuitry 902, whether external to the integrated circuit or configured on the integrated circuit as BIST circuitry, is loaded with a data test pattern (alternating 0s and 1s, for example) at terminal 904 so that the tester can expect a particular data output for a particular memory address. The skilled artisan will also appreciate that the test circuitry can generate the test pattern data as needed, rather than retrieve a stored test data pattern as described above. The memory circuit 900 is loaded with the same data pattern that is either generated by or loaded into the test circuitry along line 901.

In one approach, the frequency of the clock signal on line 906 supplied by the test circuitry to the memory circuit 900 and to the latches 908 associated with each output terminal of the memory circuit is then set to toggle at a frequency low enough to ensure that the falling

edge of the clock signal occurs after the access time has elapsed, as in the situation described above in Figure 7a. Alternatively, the test circuitry could set the duty cycle of the clock signal to ensure that the falling edge occurs after the access time has elapsed. As the test circuit reads the Lout data from the latches at terminals 910, it compares that output data to the test pattern loaded prior to the test or to the pattern generated by the test circuit itself. Since the clock frequency is relatively low or the duty cycle relatively long the output data should correspond at a given point in the clock cycle (t_M) with the data expected for the addresses chosen by the test circuitry because the access time of the memory circuit is less than the duration of the clock pulse (see Figure 7a). As the clock frequency is increased or the duty cycle decreased, however, the pulse length begins to approach the access time of the memory. When this occurs, the Lout data from the latch differs from the Dout data (see Figures 8b and 8c). The access time of the memory can them be determined from the pulse width or clock frequency at which the difference in Dout and Lout occurred.

This approach to access time measurement requires no complex control circuitry. The same clock signal is used for both the memory module operation and the Dout latch operation. No additional clock or accompanying circuitry is required as is the case with prior art approaches. Thus, test overhead on the integrated circuit is kept to a minimum and problems with differing delays between clock signals are avoided. In addition, no extra package pins or terminals are required.

The embodiments described above relate to a memory circuit embedded in an integrated circuit with a complex logic circuit. The same concepts can of course be applied to a discrete memory integrated circuit. Another preferred embodiment in accordance with the invention is shown in Figure 10. Figure 10 is a block diagram of a 256 Mb synchronous DRAM having memory cells arranged in four banks 1000. The control and addressing of the DRAM is performed by control circuit block 1002. Latency, burst length, and data output format is controlled by the mode register 1004. In this embodiment, the output 1006 is thirty-two bits wide. The access-time test approach applied in the embodiments above is also applied here. Associated with each of the thirty-two output lines 1008 (shown in Figure 10 as a single line for simplicity) is a latch 1010, and a test terminal 1012. A buffer driver 1014 may also be included to enhance the output signals. Only one set of the latch, test terminal, and buffer drive is shown in Figure 10, but it should be noted that each output line is coupled to a similar set of circuit elements. The clock signal that controls the operation of the memory circuit at terminal 1016 is coupled by line 1018 to latch 1010 to synchronize the latching of output data with memory operation. The access time test is performed as described above with reference to the embedded memory circuit.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description.

Claims

1. A circuit for measuring the access time of a memory circuit, comprising:

   a storage element having an input terminal, coupled to an output of said memory circuit;
   a clock signal source coupled to a clock terminal of said storage element and to a clock terminal of said memory circuit; and
   test circuitry coupled to address and control terminals of said memory circuit and to an output terminal of said storage element, said test equipment operable for storing or generating a test data pattern and for comparing said pattern to data output from said storage element.

2. The circuit of Claim 1, wherein said test circuitry comprises integrated on a semiconductor die with said memory circuit.

3. The circuit of Claim 1 or Claim 2, wherein said memory circuit is a dynamic random access memory circuit.

4. The circuit of Claim 1 or Claim 2, wherein said memory circuit comprises a static random access memory circuit.

5. The circuit of any preceding Claim, wherein said memory circuit comprises a non-synchronous output.

6. The circuit of any preceding Claim, wherein said storage element comprises a latch.

7. The circuit of Claim 6, wherein said latch comprises a clock-enabled inverter connected in series with a flip-flop.

8. The circuit of Claim 7, wherein said flip-flop forms a cross-coupled inverter storage cell.

9. An integrated circuit, comprising:

   control circuitry arranged to be coupled to a memory cell array;
   a clock signal input terminal arranged to be coupled to said control circuitry;
   a plurality of output terminals arranged to be

coupled to said memory cell array;
a plurality of storage elements arranged to be coupled to each of said output terminals; and
a test terminal arranged to be coupled to each of said storage elements.

10. The integrated circuit of Claim 9, wherein said storage element comprises a latch.

11. The integrated circuit of Claim 10, wherein said latch comprises a clock-enabled inverter connected in series with a flip-flop.

12. The integrated circuit of Claim 11, wherein said flip-flop forms a cross-coupled inverter storage cell.

13. The integrated circuit of any of Claims 9 to 12, further comprising a microprocessor, arranged to be coupled to said control circuitry and to said plurality of output terminals.

14. The integrated circuit of any of Claims 9 to 13, further comprising a digital signal processor, arranged to be coupled to said control circuitry and to said plurality of output terminals.

15. A method of measuring the access time of a memory circuit, comprising the steps of:

coupling a storage element to an output of said memory circuit;
providing a clock signal to said memory circuit and to said storage element;
storing a test data pattern in said memory circuit;
retrieving said test data pattern from said memory circuit by operating said memory circuit and said latch with said clock signal; and
comparing said retrieved data pattern with a second data pattern.

16. The method of Claim 15, wherein said step of comparing said retrieved data pattern comprises comparing said retrieved data pattern with second data pattern that is stored externally to said memory circuit.

17. The method of Claim 15, further comprising the step of:

generating said second data pattern during said step of comparing said retrieved data pattern with said second data pattern.

18. The method of any of Claims 15 to 17, further comprising the steps of:

retrieving said test data pattern at a clock frequency such that said retrieved test data pattern substantially matches said second data pattern; and
increasing said clock frequency such that said retrieved test data pattern substantially does not match said second data pattern.

19. The method of any of Claims 15 to 18, further comprising the steps of:

retrieving said test data pattern at a clock duty cycle such that said retrieved test data pattern substantially matches said second data pattern; and
decreasing said clock duty cycle such that said retrieved test data pattern substantially does not match said second data pattern.

20. The method of any of Claims 15 to 19, wherein said step of coupling a storage element to an output of said memory circuit comprises coupling a latch to an output of said memory circuit.

21. The method of Claim 20, wherein said step of coupling said latch comprises coupling a circuit comprising a clock-enabled inverter in series with a flip-flop to an output of said memory circuit

22. The method of Claim 21, wherein said step of coupling said circuit comprising a clock-enabled inverter in series with a flip-flop comprising coupling a circuit comprising a clock-enabled inverter in series with a cross-coupled inverter storage cell.

FIG. 1

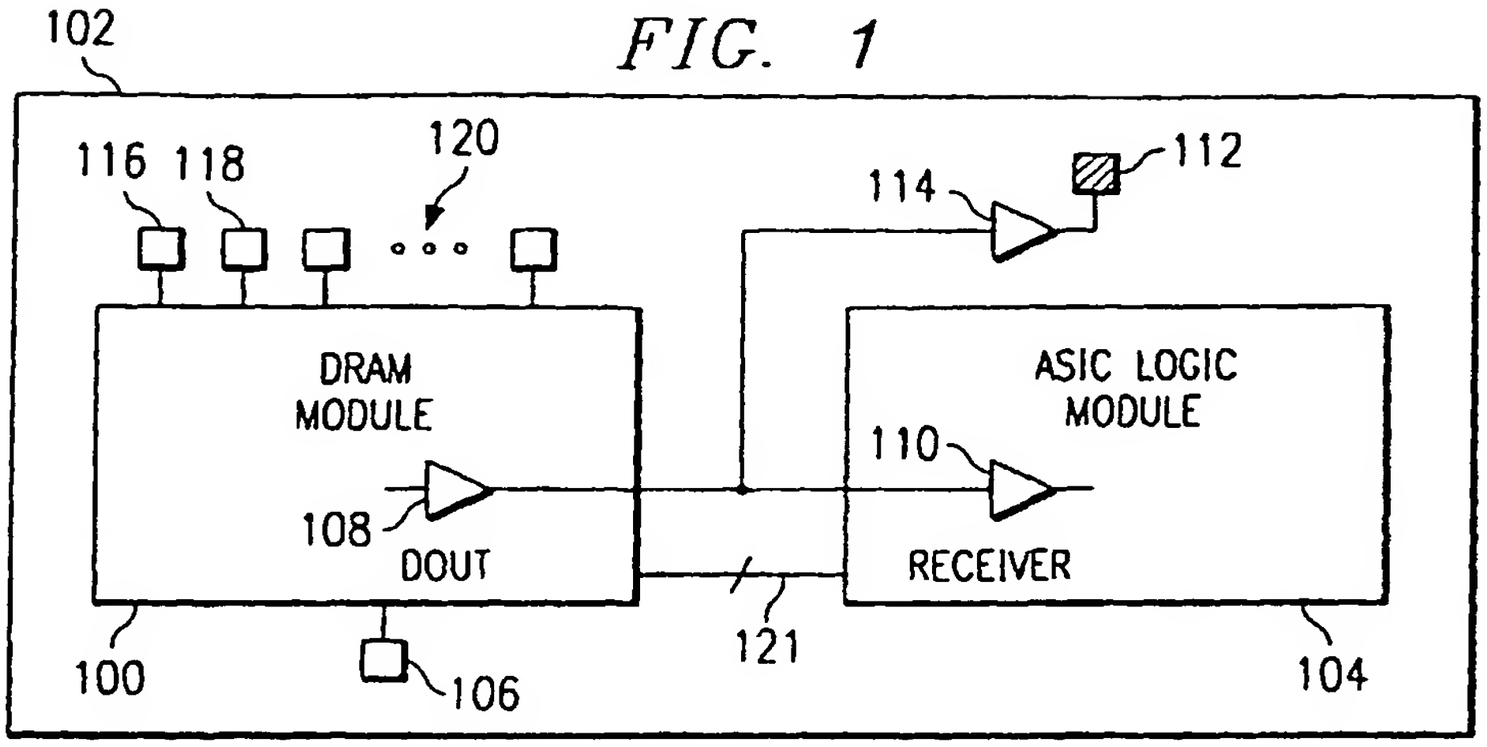


FIG. 2

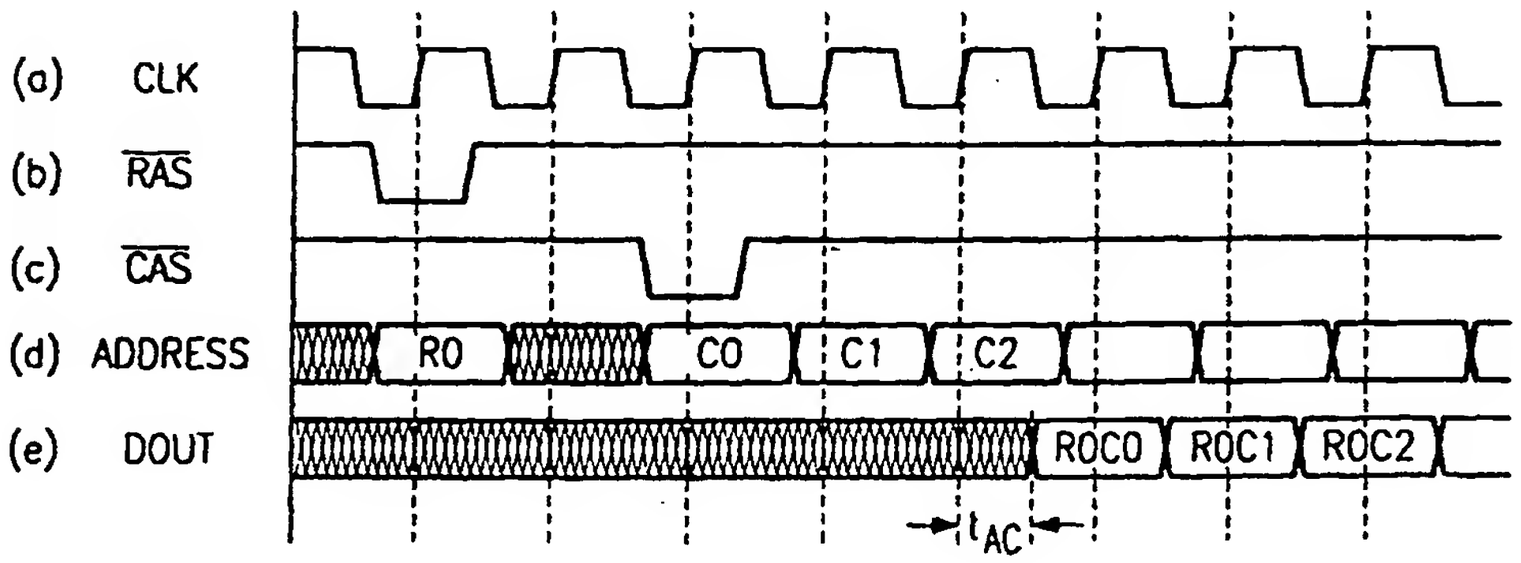


FIG. 3

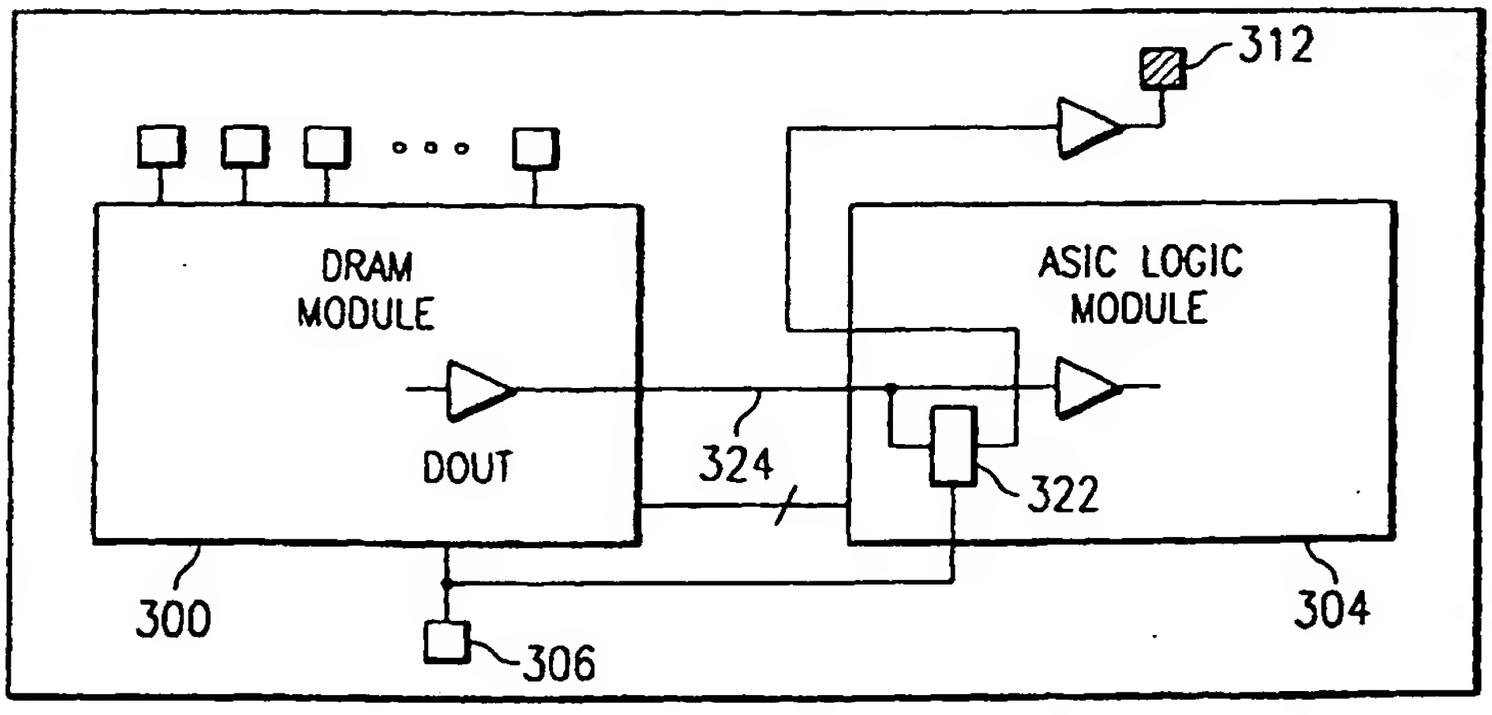


FIG. 4

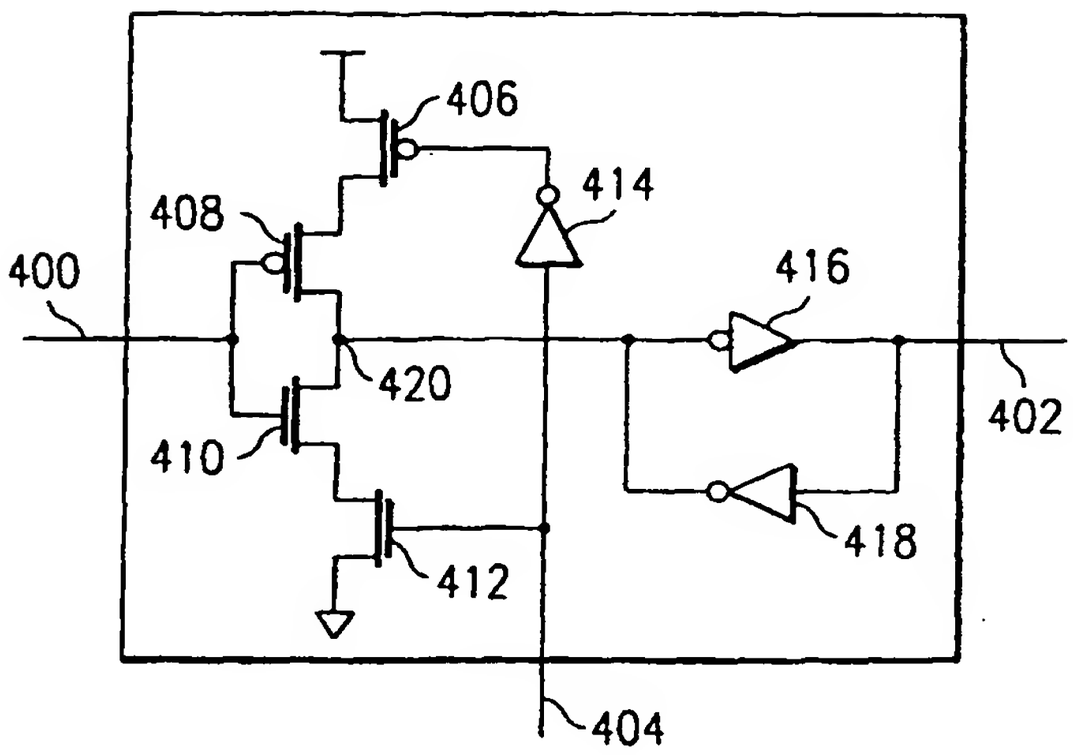

406
414
408
400
416
420
402
410
418
412
404

FIG. 5

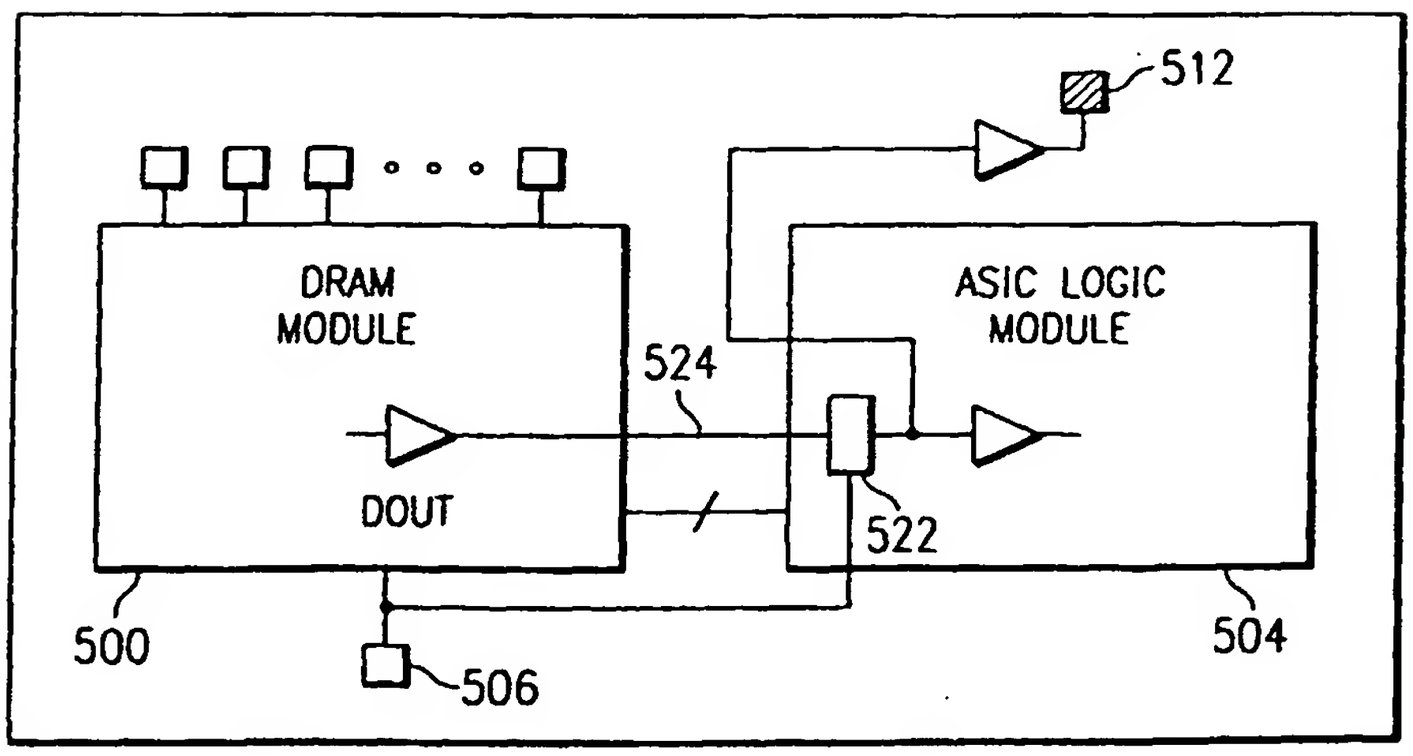

512
DRAM
MODULE
ASIC LOGIC
MODULE
524
DOUT
522
500
504
506

FIG. 6a

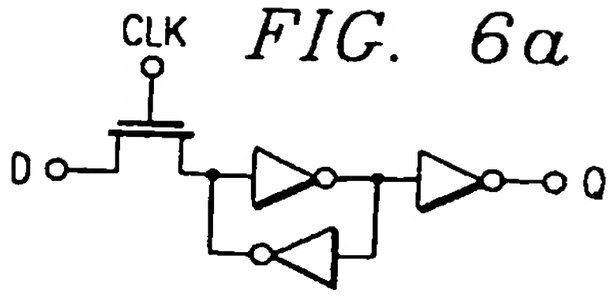


FIG. 6b

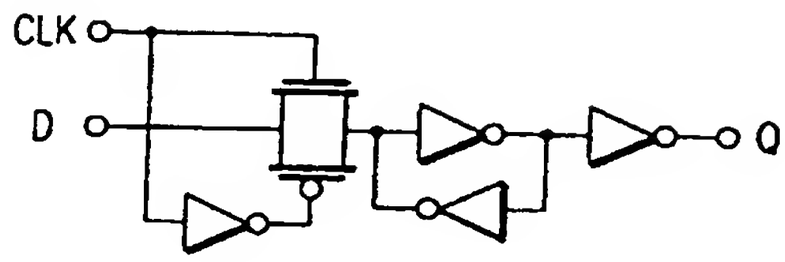


FIG. 6c

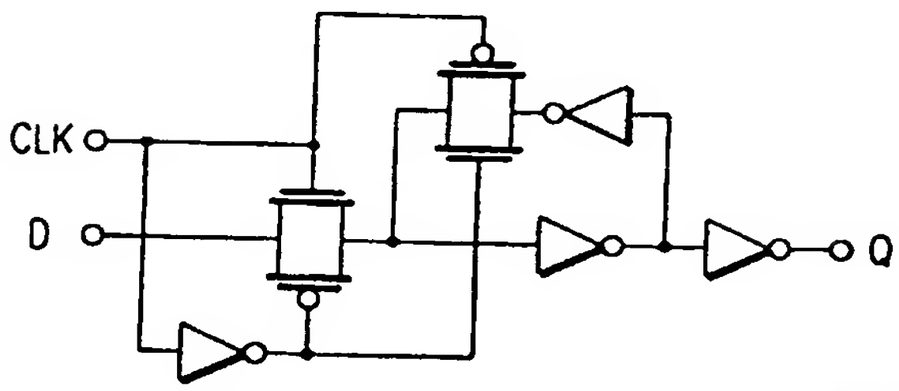


FIG. 6d

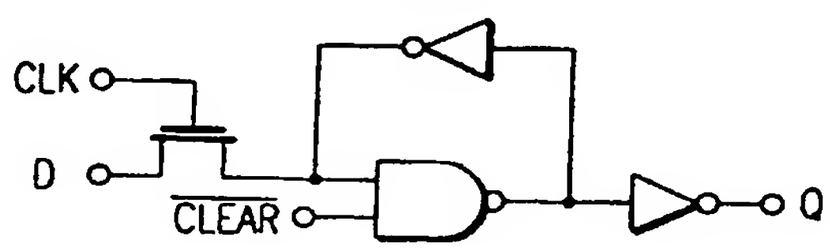


FIG. 6e

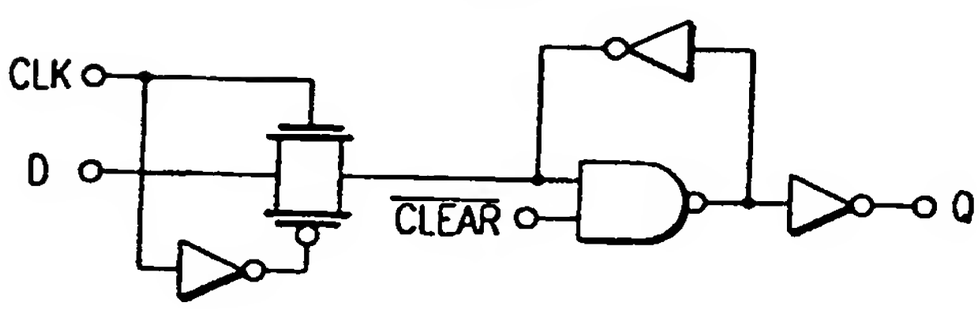


FIG. 6f

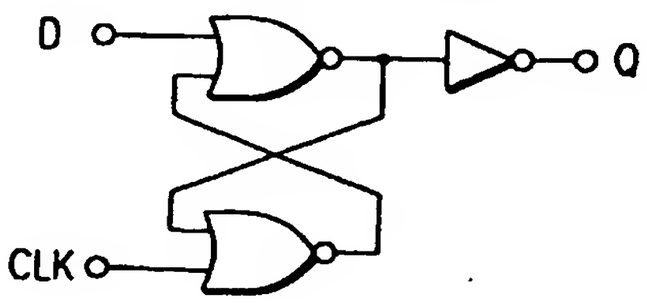


FIG. 7a

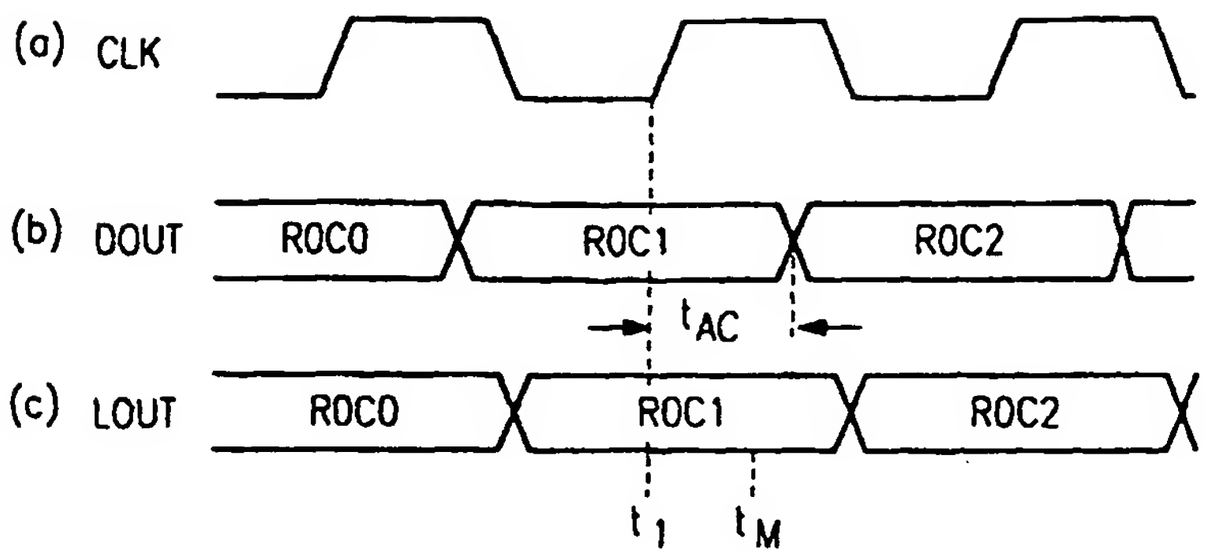


FIG. 7b

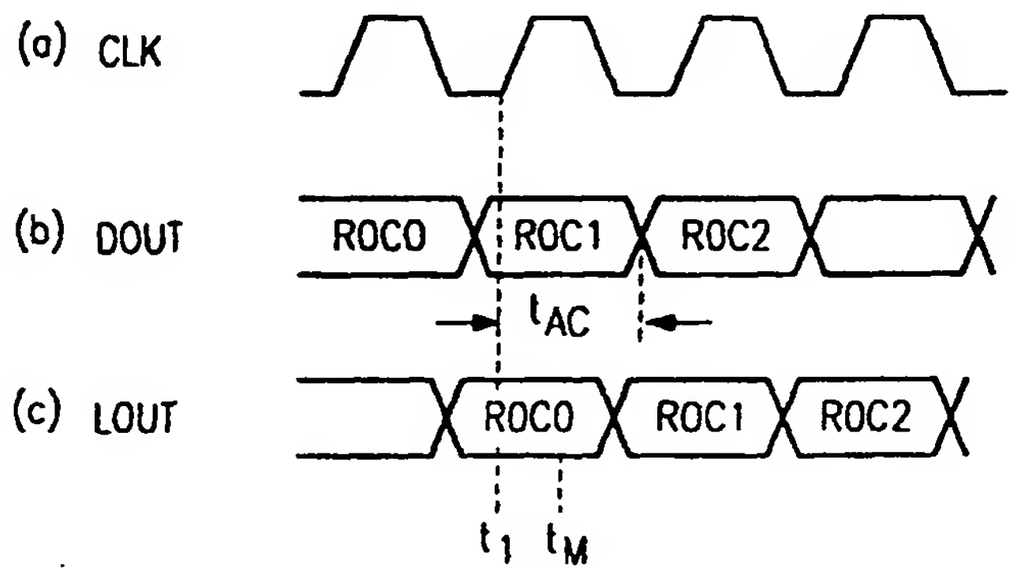


FIG. 7c

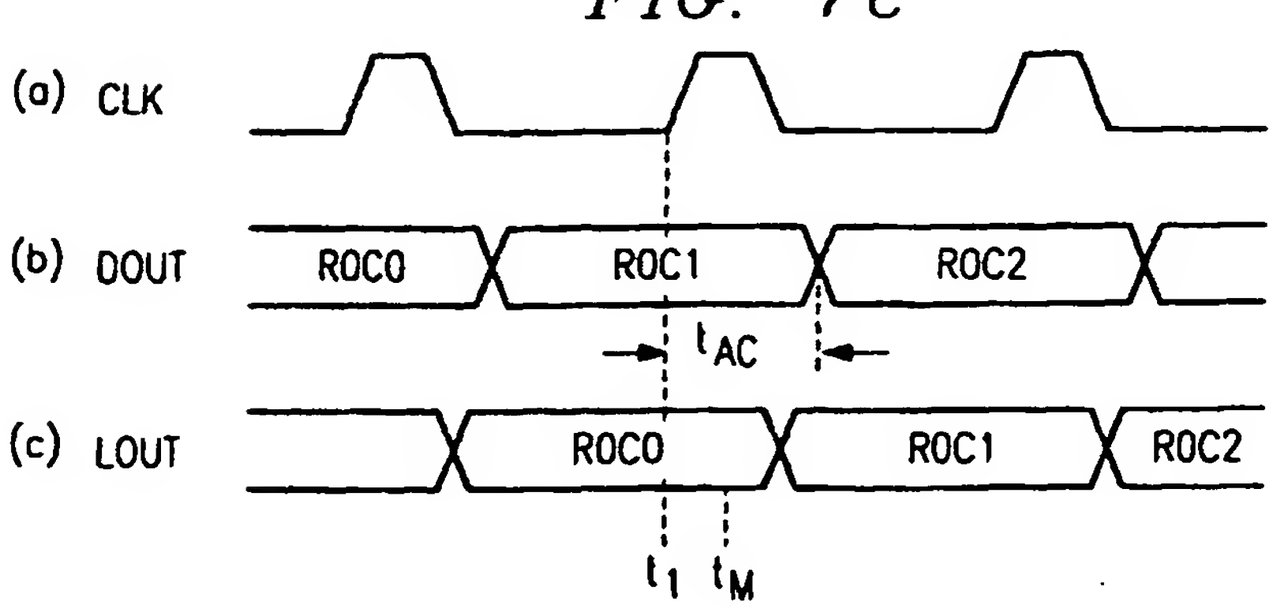


FIG. 8a

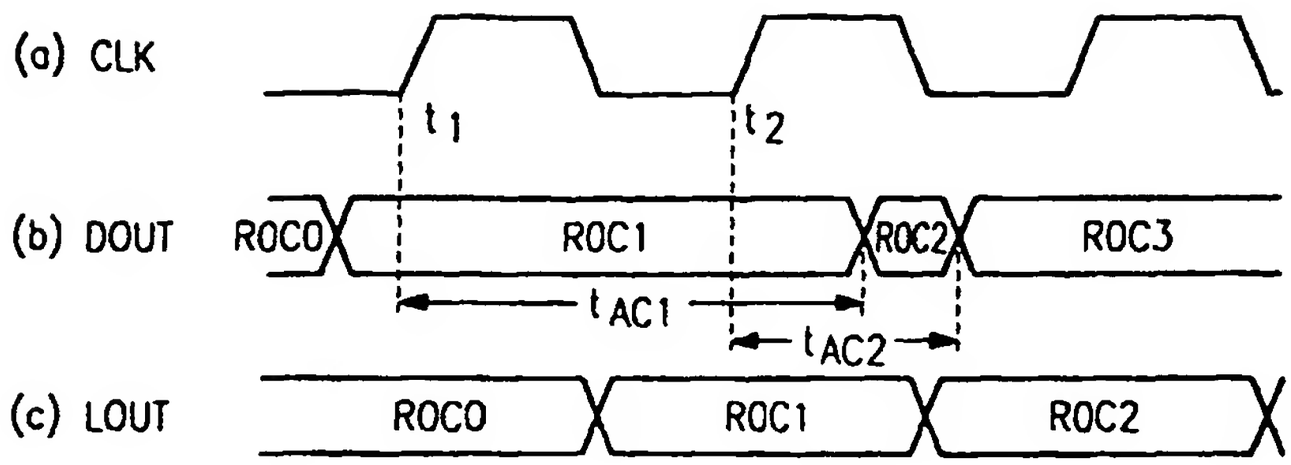


FIG. 8b

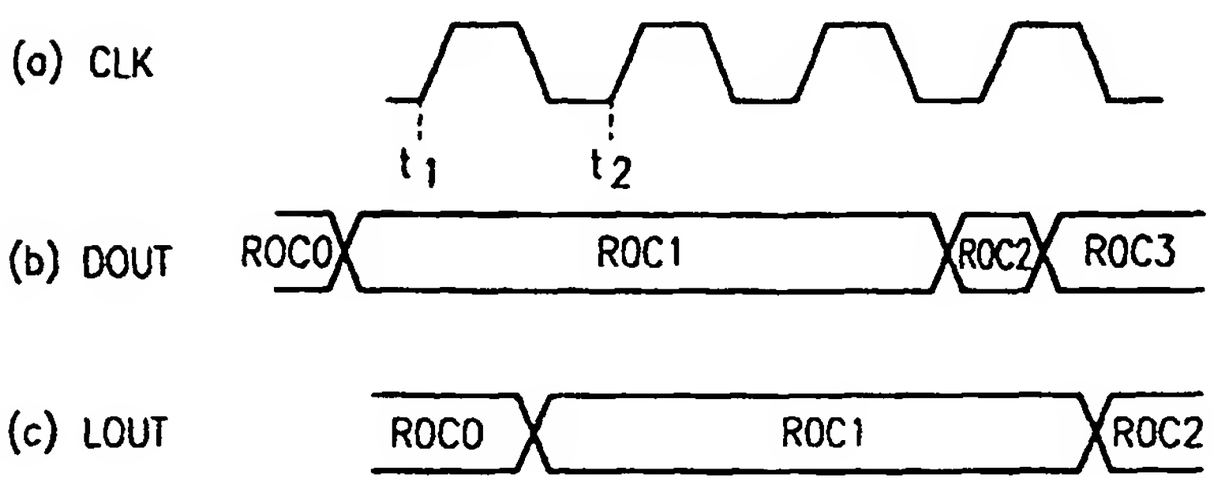
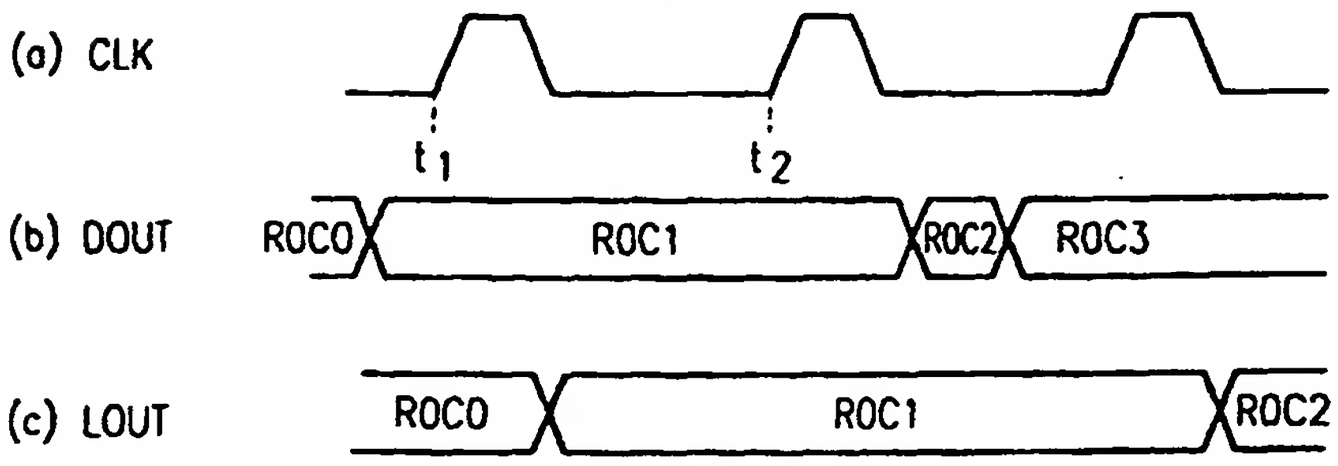


FIG. 8c



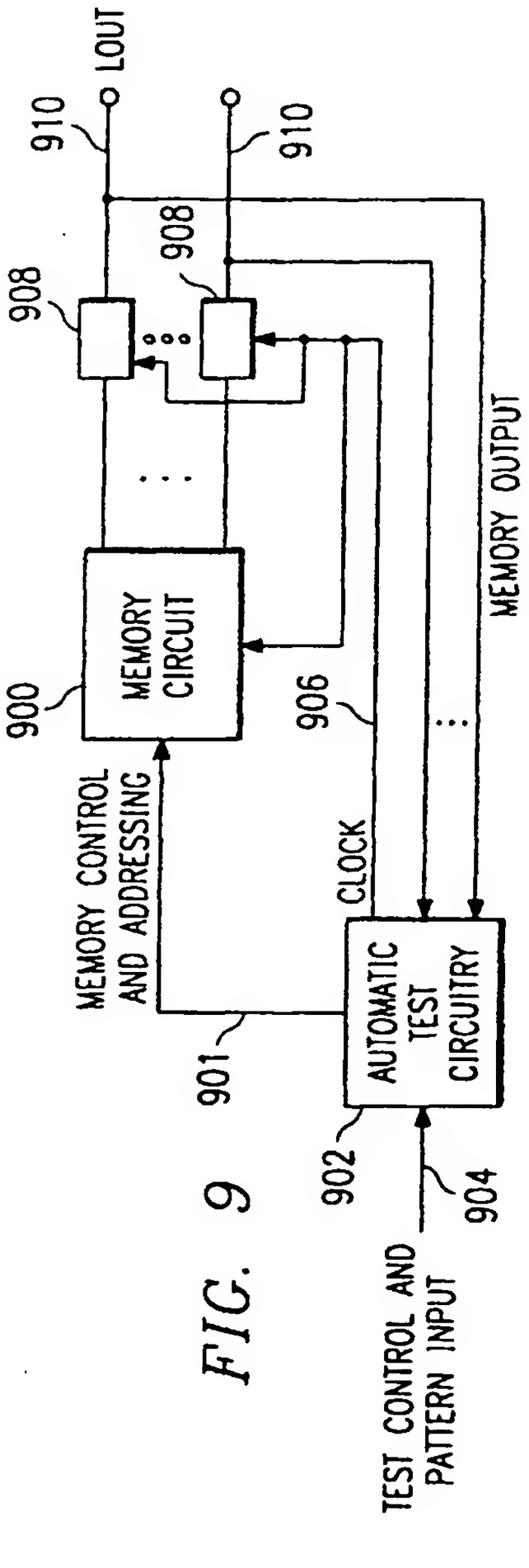

900
MEMORY CIRCUIT
908
910
LOUT
MEMORY OUTPUT
906
CLOCK
MEMORY CONTROL AND ADDRESSING
901
AUTOMATIC TEST CIRCUITRY
902
904
TEST CONTROL AND PATTERN INPUT

FIG. 9

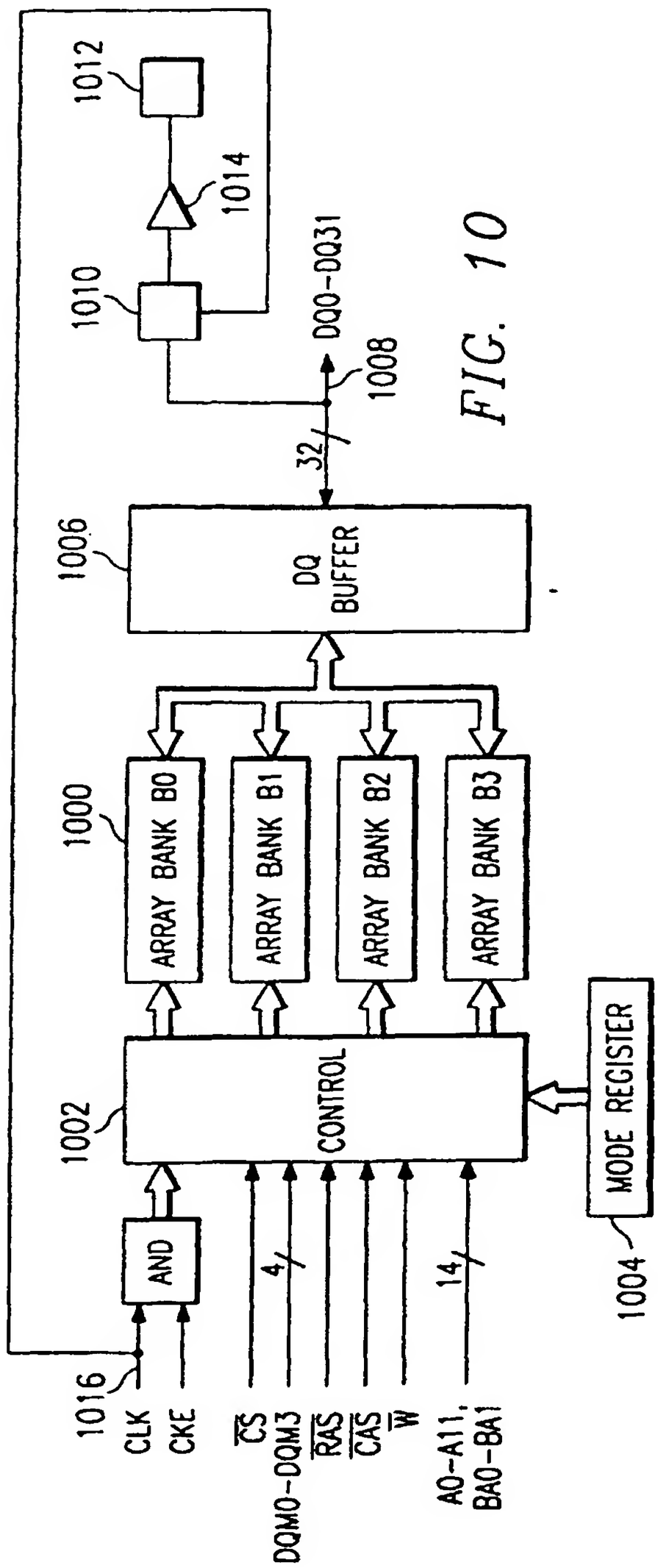

1012
1014
1010
1008
DQ0-DQ31
32
1006
DQ BUFFER
1000
ARRAY BANK B0
ARRAY BANK B1
ARRAY BANK B2
ARRAY BANK B3
1002
CONTROL
AND
MODE REGISTER
1004
1016
CLK
CKE
CS
DQM0-DQM3
RAS
CAS
W
A0-A11, BA0-BA1

FIG. 10

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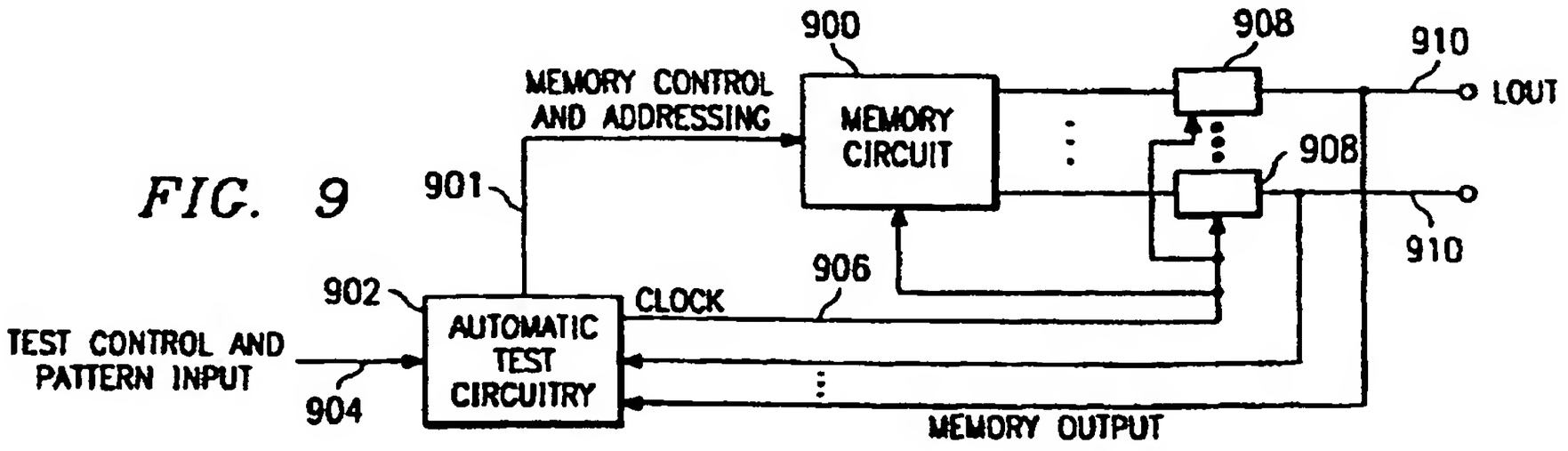
(54) Memory access time measurement circuit and method

(57) A circuit for measuring the access time of a memory circuit. The circuit includes a storage element 908 having an input terminal, an output terminal, and a clock terminal. The input terminal of the storage element is coupled to an output of the memory circuit 900. A clock signal source 906 is coupled to the clock terminal of the storage element and to a clock terminal of the memory circuit. The circuit also includes test circuitry 902 coupled to address and control terminals of the memory circuit and to the output terminal of the storage element. The test circuitry is operable to store or generate a test data pattern and compare the pattern to data output from the storage element. In one embodiment, the storage element is a data latch comprising a clock-enabled inverter serially coupled with a flip-flop. The flip-flop in one embodiment is a cross-coupled inverter storage cell or "keeper". For a clock signal having a pulse length or duty cycle that is longer than the access time of the memory circuit, the output of the storage element matches the data pattern stored by the test circuitry. As the clock frequency is increased, or the duty cycle decreased, so that the pulse length approximates the access time, the data output from the storage element no longer matches the data expected by the test circuitry, thus allowing a determination of the access time.

FIG. 9



EP 0 867 887 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 98 10 3271

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 260 982 A (FUJITSU LTD) 23 March 1988 * abstract; figure 2 * * column 1, line 32 - column 2, line 11 * * claims 1-4 *	1-22	G11C29/00
X	US 4 965 799 A (GREEN GEORGE D ET AL) 23 October 1990 * abstract; claims 1-7; figure 1 *	1-22	
A	DE 37 00 251 A (HITACHI LTD) 9 July 1987 * abstract; claims 1-6; figure 4 * * column 4, line 29 - line 56 *	1-22	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C
G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 September 1998	Sarasua Garcia, L

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